REMARKS

Examiner has rejected Claims 1-5 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that applicant regards as the invention. Examiner denotes the following terms as lacking antecedent basis: "the command", "the network", and "the succeeding time interval". Applicants have amended the claims to properly ensure each term has a proper antecedent basis.

Examiner has also pointed out claim language that is indefinite: "a global exchange", "control information communications", "a strobe interval", and "a total exchange". Applicants have amended the claims to properly define and consistently use the terms proffered.

Examiner has rejected Claims 1-5, now pending in the application, under 35 U.S.C. 103(a). Specifically, Claims 1 and 3 are rejected as being unpatentable over Raz et al. (U.S. Patent 6,173,306) in view of Kato et al. (U.S. Patent 5,600,843). Raz et al., [col. 5, line 64-col.6, lines 1 and 5-29] teaches an individual host processor, that monitors its workload, is periodically polled by a managing host processor to report the accumulated counts accumulated in each individual host processor, where the frequency of the polling is flexibly determined. Examiner states that although Raz et al. does not teach that each processor is informed by all of the other processors, a disclosed rebalancing routine by the managing host processor is essentially equivalent.

Applicants reject this assumption and respectfully traverse. The addition of a managing host processor defeats the claimed increased efficiency of applicant's invention. This is because the addition of a managing host processor into the flow scheme of information adds communication and scheduling overhead on a per-message basis that applicant's invention seeks to remove (reference applicant's page 6, lines 8-9). It is significant to note that Raz et al. teaches *monitoring* and *reporting* a processor's workload; it does *not* teach providing a priori information about the entire global state of the machine to each individual processor.

While Examiner further states that Kato et al. teaches a systolic array system that allows synchronous communications among processor elements, Applicants

submit that there is no teaching or suggestion that these communications are buffered and then globally distributed at a time certain (strobe interval). Applicant's stress that it is the buffering of control information coupled with global distribution, without the negative aspects of including a managing host processor, which provide the improvements of Applicant's invention. There is no teaching or suggestion in either Raz et al. or Kato et al. to structure communications in this way.

Further, systolic arrays pass operands of a calculation from processor element to processor element; they do *not* pass information about the state of the machine so as to optimally schedule computing resources. Furthermore, while systolic arrays are static in nature, i.e., once the array has been established, it cannot change, buffered coscheduling changes as the needs of the system change on a per time-slice basis. Therefore, it would *not* have been obvious to one of an ordinary skill in the art to combine the teachings of Raz et al. with the teachings of Kato et al. to result in Applicant's claimed invention.

As it is believed that independent Claim 1 is allowable then Examiner's rejection of dependent Claims 2, 4-5 are allowable as well. Therefore, the Examiner is requested to allow Claims 1-5, and to pass this case to issue.

Applicant's attorney would be pleased to further discuss this matter by telephone with the Examiner if the Examiner concludes such a discussion would assist in moving this case to issue. No new matter has been added as a result of this response.

Respectfully submitted,

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